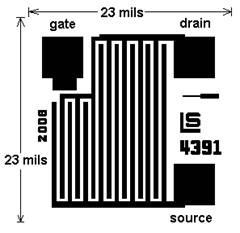
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.023”**



**G D**

**S**

**.023”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: 4391**

**APPROVED BY: DK DIE SIZE .023” X .023” DATE: 11/30/20**

**MFG: LINEAR SYSTEMS THICKNESS .017” P/N: J177**

**DG 10.1.2**

#### Rev B, 7/1